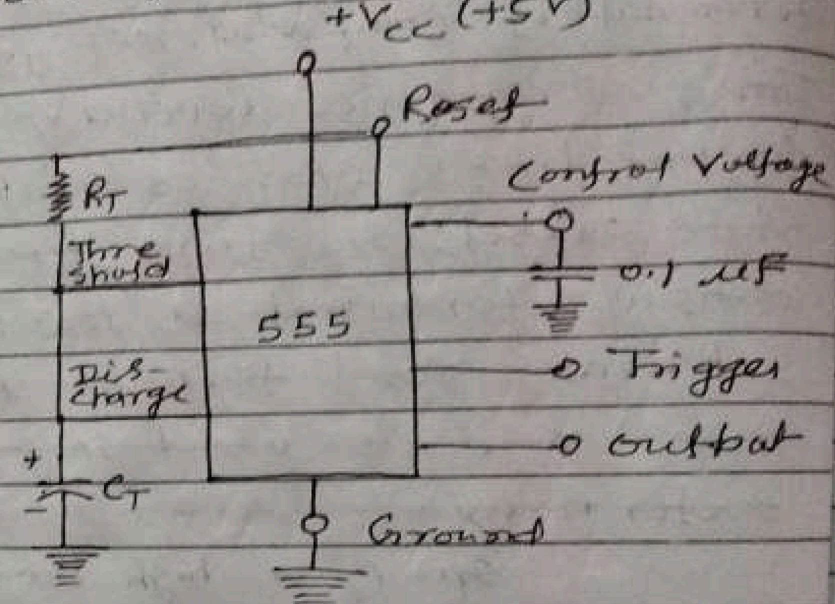
8. Timer as Monostable Multivibrator

Circuit of fig ② is to be triggered externally for monostable mode of operation. We note that :



fig(2) 555 timer.

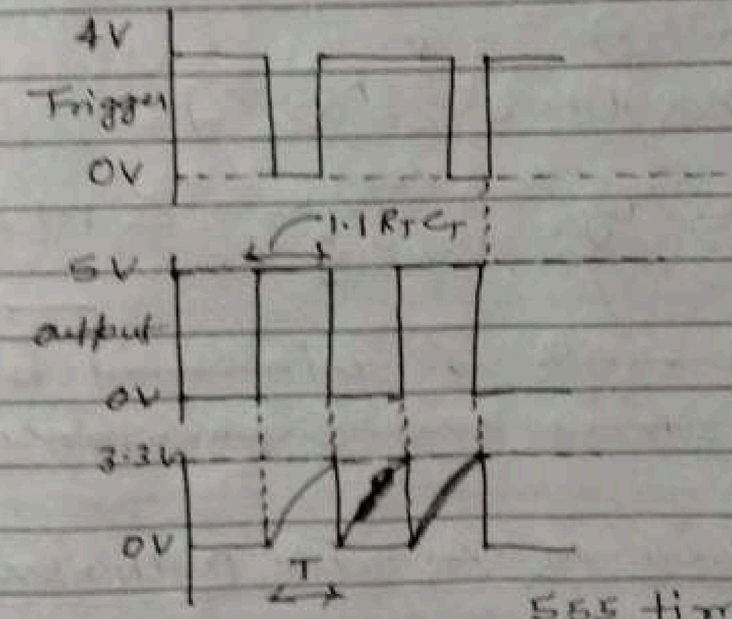
1.) When no trigger input is applied, capacitor C_T is held in the discharged state. In this case output is low.

2) When trigger input is applied and as the trigger voltage passes through $V_{cc}/3$ (threshold level of comparator - 2), comparator - 2 changes its output state so that flip-flop is set, i.e. $\overline{Q} = 0$ and transistor Q_1 becomes OFF. Therefore timing cycle begins, i.e. capacitor C_T charges up exponentially through R_T towards V_{cc} with time constant $R_T C_T$ according to

$$V_c = V_{cc}(1 - e^{-t/R_T C_T}) \longrightarrow ①$$

where V_c is the voltage across the capacitor at any time t.

3). When this voltage V_c, reaches $2V_{cc}/3$ (threshold level of comparator-1), as it is connected to threshold terminal, comparator-1 changes its output state so that flip-flop is reset,



555 timer used as a one shot multivibrator

fig-(3)

Note
$V_c = 2\frac{V_{cc}}{3} = 2\times\frac{5}{3} = 3.3$ V

i.e. $\bar{Q} = 1$. This makes the transistor Q_1, ON and the capacitor discharges rapidly to ground; the timing cycle is completed.

once The Circuit is triggered, it is insen-sitive to further triggering Pulses until The timing cycle is Completed.

4.) From Point (2) & (3) we note That time Period of The timing Cycle is The time required for The Capacitor to Charge from Zero to $2V_{cc}/3$. This Period Can be obtained on Putting $V_c = 2V_{cc}/3$ at $t = T$ in eqn (1). i.e.

$$2V_{cc}/3 = V_{cc}(1 - e^{-T/R_T C_T})$$

$$T = R_T C_T \log_e \frac{V_{cc}}{V_{cc} - \frac{2}{3}V_{cc}} \cong 1.1 R_T C_T \quad \text{--- (2)}$$

Thus Pulse width is determined by external resistance and Capacitance.

⟨B.⟩ Timer used as Astable Multivibrator:-

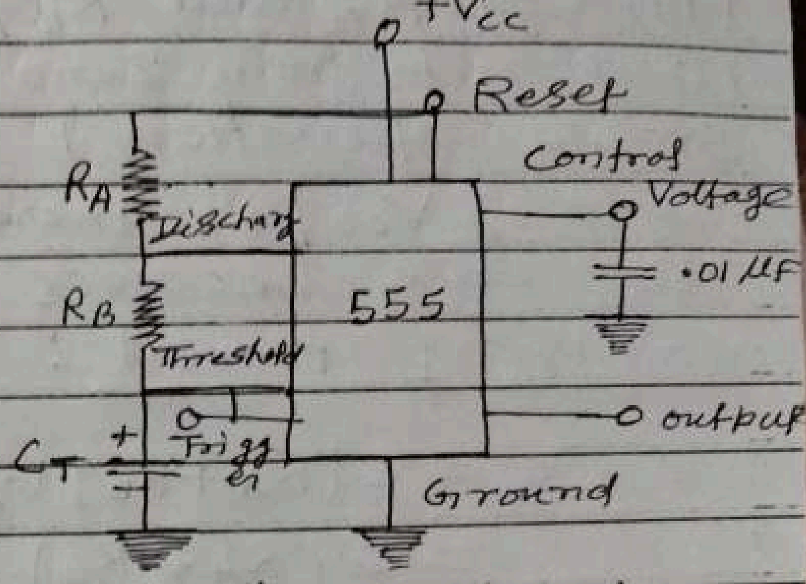
External Connections for astable operation are shown in fig (4). For This operation Circuit does not require any external trigger Signal; Therefore, trigger terminal is Connected to Threshold terminal So That at all time V_c, is applied to both these inputs. Further, two series resistors R_A & R_B

VKSU

are also used, whose common junction is connected to discharge terminal. Its operation is as follows :

Operation :-

During charging up period transistor Q_1 is held open by the flip-flop and capacitor charges through series connected resistors R_A and R_B when voltage across capacitor reaches $2V_{cc}/3$ (reference



fig(4) 555 timer: External connection for astable operation

level of comparator-1) comparator-1 changes its output state and it changes the state of flip-flop so that transistor Q_1 is now ON. The capacitor then discharges through R_B until its voltage drops to $V_{cc}/3$ (reference level of comparator-2). This comparator then changes the state of flip-flop again which, in turn, makes the transistor Q_1 OFF and thus the cycle repeats itself.

VKSU

Charging Period :- As is clear from above description, charging of the capacitor (Through R_A and R_B) starts from Vcc/3 (and not from zero as in case of mono-stable operation) and continues upto 2Vcc/3. Therefore eqn (2) for This case becomes :

Charging Period :

$$T_1 = C(R_A + R_B) \log_e \frac{V_{cc} - V_{cc}/3}{V_{cc} - 2V_{cc}/3}$$

$$= C(R_A + R_B) \log_e 2$$

$$= 0.7(R_A + R_B) C$$

Discharge Period : capacitor discharges (Through R_B only) from 2Vcc/3 towards zero volt. This discharge is terminated at Vcc/3 at which comparator - 2 changes state. Hence discharge period is determined by the equation

$$T_2 = C R_B \log_e \frac{0 - 2V_{cc}/3}{0 - V_{cc}/3} = 0.7 R_B C.$$

Total Period : $T = T_1 + T_2 = 0.7(R_A + 2R_B) C$

Charging and discharging intervals differ by $0.7 R_A C$.